The timing characteristics of Synchronous Sequential Circuits are discussed in this tutorial. We will begin with the general concepts associated with timing and then will proceed with examples to better understand their application to digital design. This tutorial consists of three sections.

PART 1: Introduction and terminology

A Digital System Design circuit can be characterized as a 'Combinational circuit' or a 'Sequential Circuit' and while calculating for Timing we will have to first identify what type of circuit is involved.

Q1. How do we know whether a given circuit is a Combinational Circuit or a Sequential Circuit?

[Ans] If a circuit has only combinational devices (e.g. gates like AND, OR, MUX(s), etc.) and no Memory elements then it is a Combinational circuit. If the circuit has memory elements such as Flip Flops, Registers, Counters, or other state devices then it is a Sequential Circuit. Synchronous sequential circuits will also have a clearly labeled clock input.
Q2. Are the following circuits combinational or sequential?

[Ans]

Q3. Why do we have to identify the type of circuit? Does it really matter?

[Ans] It is important to identify the type of circuit because the timing characteristics differ. Combinational circuit timing analysis deals primarily with propagation delay. Sequential circuits have additional timing characteristics that must be satisfied in order to prevent metastability, including setup time, hold time, and minimum clock period. Designers of sequential devices must specify these important timing characteristics in order to allow the device to be used without error.

Q4. Do all Digital Devices like gates and Flip Flops have timing parameters?

[Ans] Yes, all “real” digital devices have timing characteristics that must be obeyed in order for the device to function is it is intended.
Q5. What makes propagation delay important to know/understand?

[Ans] All real devices have some delay associated with transferring an input change to the output. Although a ideal gate doesn’t have such a delay, any implementation in the real world takes time to do its job. This delay that is due to the signal propagation through the device is called the propagation delay.
Q6. What is Setup time?

[Ans] Setup time is a timing parameter associated with Sequential Devices (for simplicity henceforth I will be only referring to the Flip Flop). The Setup time is used to meet the minimum pulse width requirement for the first (Master) latch that makes up a flip flop. More simply, the setup time is the amount of time that an input signal (to the device) must be stable (unchanging) before the clock ticks in order to guarantee minimum pulse width and thus avoid possible metastability.

Q7. What is Hold time?

[Ans] Hold time is also a timing parameter associated with Flip Flops and all other sequential devices. The Hold time is used to further satisfy the minimum pulse width requirement for the first (Master) latch that makes up a flip flop. The input must not change until enough time has passed after the clock tick to guarantee the master latch is fully disabled. More simply, hold time is the amount of time that an input signal (to a sequential device) must be stable (unchanging) after the clock tick in order to guarantee minimum pulse width and thus avoid possible metastability.
Q8. What do Setup and Hold time look like on a timing diagram?

[Ans] Observe the waveform below:

The timing diagram above illustrates three signals: the Clock, the Flip Flop Input (D) and the Flip Flop output (Q).

(1) is the Setup Time \([t_2 - t_1]\): the minimum amount of time Input must be held constant BEFORE the clock tick. Note that D is actually held constant for somewhat longer than the minimum amount. The extra “constant” time is sometimes called the setup margin.

(2) is the Propagation delay of the Flip Flop \([t_3 - t_2]\): this is the time that it takes for the new input to be to propagate and influence the output.

(3) is the Hold time \([t_4 - t_2]\): the minimum amount of time the Input is held constant AFTER the clock tick. Note that Q is actually held constant for somewhat longer than the minimum amount. The extra “constant” time is sometimes called the hold margin.

(The above timing diagram has 2 clock cycles; the timing parameters for the second cycle will also be similar to that of the first cycle)
PART 2: Equations

This part of the tutorial introduces us to the various different timing calculations associated with this course. We may be given a sequential circuit and asked to solve for the timing parameters. Let us discuss in detail how we should approach such problems.

Q21. What is the first thing to do if given a sequential circuit and asked to analyze its timing?

[Ans] For the purposes of understanding the “big picture”, consider a circuit divided into three distinct parts: Next-State Logic, State Memory and Output Logic. The Next State Logic and the Output Logic blocks consist of only combinational logic components (gates, muxes, etc.) The state memory block is made of only sequential components (flip-flops, registers, etc.)

A given sequential circuit can be represented in either of the two ways as shown below.

The first representation shows the sequential circuit where the input(s) have to pass through the State memory to affect the output. Such machines are called Moore machines.
The second representation shows the ‘red bypass’ which signifies that the output can be directly affected by the inputs without having to pass through the state memory device(s). Such devices are called Mealy machines.

Q22. Can you explain this with an example?

[Ans] Ok, consider the sequential circuit shown below

Let us now identify the three distinct parts in this given sequential circuit. Observe the division on the circuit below.

Observation: This given circuit is a MEALY machine.
Q23. What timing parameters are important?

[Ans] Remember from our discussion in Part 1 of this tutorial we know that combinational devices and sequential devices have different timing parameters. Now that we have separated them both into separate blocks we can define them more clearly. Let us refer to the timing parameters for the input logic (also referred to as the next state logic) and output logic with the letter ‘F’ and ‘G’ respectively. Similarly, let us refer to all timing parameters associated with the State memory block with the letter ‘R’.

**Moore Machine**
Since in this circuit (machine) the only way the input can influence the output is through the State Memory (FF) this is a Moore Machine.

The amount of time that the excitation equation has to be held constant before the clock occurs.

**Mealy Machine**
In this Machine (circuit) the input directly influences the output by bypassing the State Memory (FF) which is why this is a Mealy Machine.
Q24. What timing parameters must be provided/calculated for a synchronous sequential device?

[Ans] The list of the timing parameters that you may be asked to calculate for a given sequential circuit is

1. Propagation delay, Clock to Output (minimum)
2. Propagation delay, Clock to Output (maximum)
3. Propagation delay, Input to Output (minimum)
4. Propagation delay, Input to Output (maximum)
5. Setup Time (Data input before clock)
6. Hold Time (Data input after clock)
7. Maximum Clock rate (or its reciprocal, minimum clock period)

Q25. How do we find the Propagation delay, Clock to Output?

[Ans] Propagation delay (PD) for the circuit can be calculated as the summation of all delays encountered from where the clock occurs to the output. In short, the delays of the State memory and the output logic. In the abstract:

\[
PD_{\text{Clock-Output (min)}} = R_{pd (min)} + G_{pd (min)}
\]

\[
PD_{\text{Clock-Output (max)}} = R_{pd (max)} + G_{pd (max)}
\]

Q26. How do we find the Propagation delay, Input to Output?

[Ans] This is a property associated with Mealy machines only. In other words, for a Moore machine the value for this timing parameter is infinity (∞). The calculation (for mealy machines) is the summation of all propagation delays encountered between the input (that influences the output by bypassing the state memory) and the output.

For MOORE machines:

\[
PD_{\text{Input-Output (min)}} = \text{infinity (∞)} \quad \text{(you will also see NA, -, and/or 0)}
\]

\[
PD_{\text{Input-Output (max)}} = \text{infinity (∞)} \quad \text{(you will also see NA,-, and/or 0)}
\]
For MEALY Machines

\[
P_{D_{\text{Input-Output}}} (\text{min}) = G_{pd} (\text{min})
\]

\[
P_{D_{\text{Input-Output}}} (\text{max}) = G_{pd} (\text{max})
\]

Q27. How do we calculate Setup time?

[Ans] The calculation for setup time is the sum of the setup time for the concerned flip flop and the maximum delay from the input logic. In the abstract:

\[
T_{\text{setup}} = R_{\text{setup}} + F_{pd} (\text{MAX})
\]

Q28. How do we calculate the Hold time?

[Ans] The concern here is how soon (minimum time) a primary input can propagate a new value through the Input logic while the Flip Flop is attempting to hold on to a stable value. In the abstract, hold time is calculated with the following general formula:

\[
T_{\text{hold}} = R_{\text{hold}} - F_{pd} (\text{MIN})
\]

Note that, the minimum value for hold time is 0. If the calculation produces a negative value, we report a 0 hold time. Circuits of moderate complexity (or higher) generally have hold times of 0, and thus hold time is generally not a consideration in high-level design.

Q29. How do we calculate the Maximum Clock rate (MCLK)?

[Ans] Maximum clock rate is the reciprocal of the minimum clock period. In other words, clock ticks must be spaced out far enough that the digital device has the necessary time to fully change to its new state before it receives a new clock tick.

\[
MCLK = \frac{1}{T_{\text{MIN}}}
\]

\[T_{\text{MIN}}\] here refers to the minimum time period for correct operation of the circuit, so it is calculated using all worst cases (maximum delays). In the abstract:
\[ T_{\text{MIN}} = F_{pd}(\text{MAX}) + R_{\text{SETUP}} + R_{pd}(\text{MAX}) \]

Thus:

\[ MCLK = \frac{1}{T_{\text{MIN}}} = (F_{pd}(\text{MAX}) + R_{\text{SETUP}} + R_{pd}(\text{MAX}))^{-1} \]

---

**SUMMARY TIMING EQUATIONS**

1. \( \text{PD}_{\text{Clock-Output}} \text{ (min)} = R_{pd} \text{ (min)} + G_{pd} \text{ (min)} \)
2. \( \text{PD}_{\text{Clock-Output}} \text{ (max)} = R_{pd} \text{ (max)} + G_{pd} \text{ (max)} \)
3. \( \text{PD}_{\text{Input-Output}} \text{ (min)} = \text{infinity} (\infty) \text{ (For MOORE machines)} \)
4. \( \text{PD}_{\text{Input-Output}} \text{ (max)} = \text{infinity} (\infty) \text{ (For MOORE machines)} \)
5. \( \text{PD}_{\text{Input-Output}} \text{ (min)} = G_{pd} \text{ (min)} \text{ (For MEALY machines)} \)
6. \( \text{PD}_{\text{Input-Output}} \text{ (max)} = G_{pd} \text{ (max)} \text{ (For MEALY machines)} \)
7. \( T_{\text{SETUP}} = R_{\text{SETUP}} + F_{pd} \text{ (MAX)} \)
8. \( T_{\text{HOLD}} = R_{\text{HOLD}} - F_{pd} \text{ (MIN)} \)
9. \( MCLK = \frac{1}{T_{\text{MIN}}} = (F_{pd}(\text{MAX}) + R_{\text{SETUP}} + R_{pd}(\text{MAX}))^{-1} \)
**Q31.** Consider the following digital device. The timing characteristics of its components are available in the table below. What are the timing characteristics of the overall device?

<table>
<thead>
<tr>
<th>Device</th>
<th>Propagation Delay (Minimum)</th>
<th>Propagation Delay (Maximum)</th>
<th>Setup Time</th>
<th>Hold Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>D Flip Flop</td>
<td>4 ns</td>
<td>8 ns</td>
<td>10 ns</td>
<td>3 ns</td>
</tr>
<tr>
<td>NAND Gate</td>
<td>3 ns</td>
<td>6 ns</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Bubbled AND Gate</td>
<td>2 ns</td>
<td>4 ns</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

**[Ans]** With this information we can approach the problem as discussed in Part 2 of this tutorial. Note that the abstract equations help GUIDE the analysis, the actual timing characteristics are dependent upon specific paths of propagation in the realized device. In this first example, the “abstract model” is sufficient. Note that this is a MEALY machine.

1. $PD_{\text{Clock-Output (min)}} = R_{pd \text{ (min)}} + G_{pd \text{ (min)}} = 4\, \text{ns} + 2\, \text{ns} = 6\, \text{ns}$
2. $PD_{\text{Clock-Output (max)}} = R_{pd \text{ (max)}} + G_{pd \text{ (max)}} = 8\, \text{ns} + 4\, \text{ns} = 12\, \text{ns}$
3. $PD_{\text{Input-Output (min)}} = G_{pd \text{ (min)}} = 2\, \text{ns}$
4. $PD_{\text{Input-Output (max)}} = G_{pd \text{ (max)}} = 4\, \text{ns}$
5. $T_{\text{setup}} = R_{\text{setup}} + F_{pd \text{ (MAX)}} = 10\, \text{ns} + 6\, \text{ns} = 16\, \text{ns}$
6. $T_{\text{hold}} = R_{\text{hold}} - F_{pd \text{ (MIN)}} = 3\, \text{ns} - 3\, \text{ns} = 0\, \text{ns}$.
7. $T_{\text{min}} = F_{pd \text{ (MAX)}} + R_{\text{setup}} + R_{pd \text{ (MAX)}} = 6\, \text{ns} + 10\, \text{ns} + 8\, \text{ns} = 24\, \text{ns}$
8. $MCLK = 1/ T_{\text{min}} = (F_{pd \text{ (MAX)}} + R_{\text{setup}} + R_{pd \text{ (MAX)}})^{-1} = 1/24\, \text{ns}$. 

[12/13]
Q32. Consider the following digital device. The timing characteristics of its components are available in the table below. What are the timing characteristics of the overall device?

<table>
<thead>
<tr>
<th>Device</th>
<th>Propagation Delay (minimum)</th>
<th>Propagation Delay (maximum)</th>
<th>Setup Time</th>
<th>Hold Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>D Flip Flop</td>
<td>2ns</td>
<td>6ns</td>
<td>4ns</td>
<td>2ns</td>
</tr>
<tr>
<td>AND Gate</td>
<td>2ns</td>
<td>4ns</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>2 i/p NOR Gate</td>
<td>2ns</td>
<td>3ns</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>OR Gate</td>
<td>2ns</td>
<td>3ns</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>3 i/p NOR Gate</td>
<td>1ns</td>
<td>2ns</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

[Ans] Note that there are multiple flip-flops, and thus potentially multiple paths that must be analyzed. Each path should be analyzed individually. The MOST constraining path is the reported timing characteristic.

1. PD Clock- Output (min) = Rpd (min) + Gpd (min) = 2ns + 1ns = 3ns
2. PD Clock- Output (max) = Rpd (max) + Gpd (max) = 6ns + 3ns + 2ns = 11ns
3. PD Input- Output (min) = Gpd (min) (For MEALY machines) = 1ns
4. PD Input- Output (max) = Gpd (max) (For MEALY machines) = 2ns
5. T SETUP = RSETUP + Fpd (MAX) = 4ns + 4ns = 8ns
6. T HOLD = RHOLD - Fpd (MIN) = 2ns - 2ns = 0ns.
7. TMIN = Fpd (MAX) + RSETUP + Rpd (MAX) = 3ns + 4ns + 4ns + 6ns = 17ns
8. MCLK = 1/ TMIN = (Fpd (MAX) + RSETUP + Rpd (MAX))^-1 = 1/17ns.

Original version of this document prepared for Dr. Doom by Sridhar Ramachandran (CEG 360/560 GTA)